OPTIMTECH

AXI4 to memory bridge with SECDEC and exclusive access support. RTL name: axi2mem.

IP datasheet

March 8, 2021

Contents

1 Block diagram

IP block diagram is presented below.

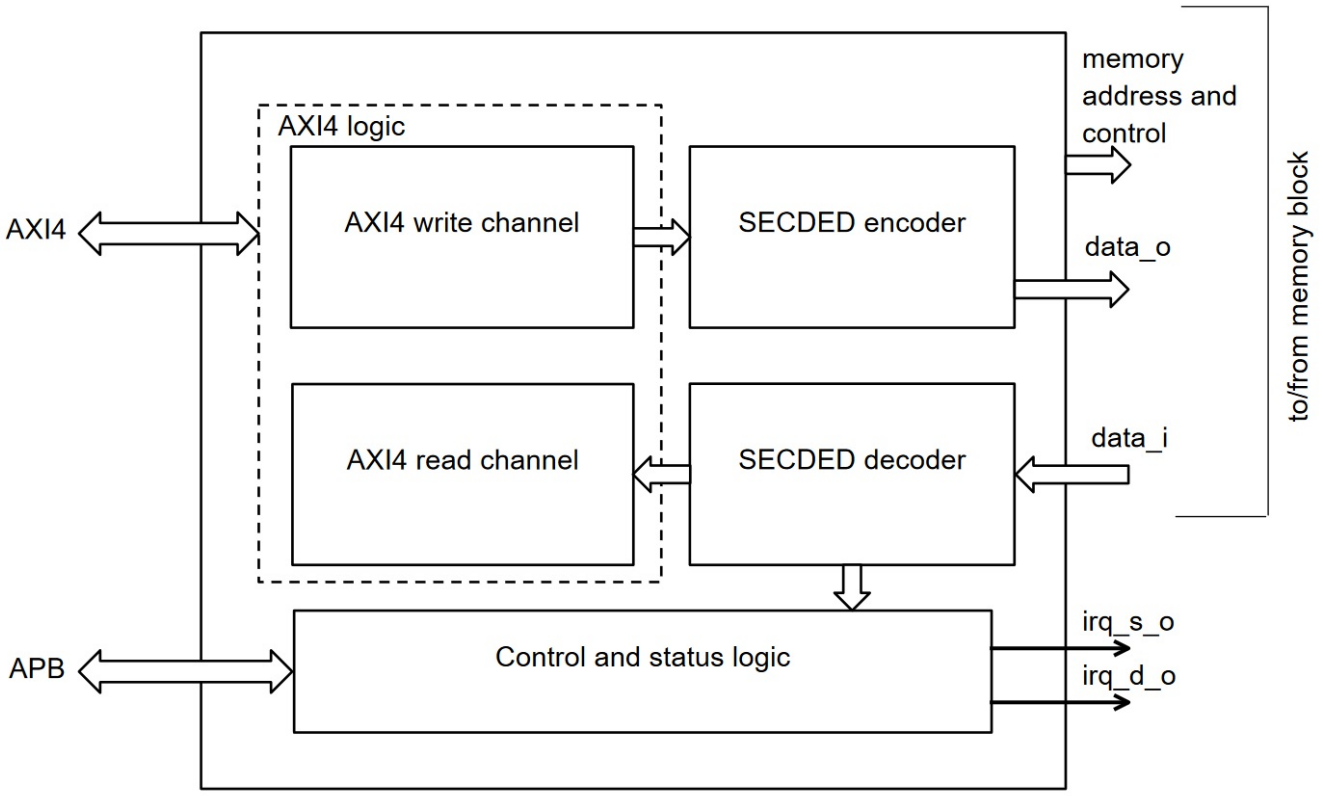

Figure 1: Block diagram

2 Functional description

2.1 Overview

axi2mem bridge should be used to connect standard RAM or ROM blocks with plain CE-WE input control interface to AXI4 bus. It supports exclusive accesses (AXI4 transactions with AxLOCK=0b1 according to AXI4 specification). Main features of axi2mem:

- supports all types and sizes of AXI4 read bursts
- supports all types and sizes of AXI4 write bursts
- supports AXI4 exclusive accesses
- configurable address and data widths
- configurable AXI4 ID width
- configurable size of connected ROM/RAM block (based on address width)
- check ROM/RAM address validity option
- SECDED option with interrupts generation and failed address storage (controlled/accessed via APB interface)

- Read-Modify-Write option to support non-byte-enable memory (this option is always enabled together with SECDED option)

2.2 SECDED

axi2mem bridge has option of SECDED encoders/decoders insertion. When this option is enabled APB interface is also added to block. APB interface can be used to enable interrupt generation and to access failed addresses values (addresses where single and double errors are detected). For more intformation see register description section of this document.

When SECDED option is enabled axi2mem uses Read-Modify-Write sequence for write transfers, where not all bytes are to be written. This means that in this case byte write enable option of RAM blocks is unnesessary and is adviced to be removed to reduce silicon area.

When SECDED option is enabled and double error occurs, the response to AXI4 read transfer (RRESP) with incorrect read data will be SLVERR.

2.3 Interrupts

axi2mem bridge can generate interrupt requests when all following conditions are satisfied:

- SECDED option is enabled
- SECDED blocks detected single/double error
- interrupt generation due to single/double error is enabled via control registers (accessed via APB)

Interrupts due to single and double errors can be enabled separately by corresponding enable bits. Interrputs are level-triggered. axi2mem invokes a level-triggered interrupt by driving the signal to and holding it at the active level. It negates the signal when the processor commands it to do so (when it clears corresponding flag in status register).

2.4 Connection to memory macro

There are 3 possible configuration cases that should be considered when connection to memory macro is established:

1. SECDED and Read-Modify-Write are disabled
2. Read-Modify-Write is enabled
3. SECDED and Read-Modify-Write are enabled

For more information about how one of these cases is selected see "Configuration options" section of this document. There are 2 possible memory macro types that should be considered:

1. memory macro without byte write enable (usually denoted as BE) inputs
2. memory macro with BE inputs

For first configuration case only memory macro with BE inputs is allowed. For configuration cases 2 and 3 both memory macro types are allowed, but when memory macro with BE inputs is used, it should be connected as shown on figure below.

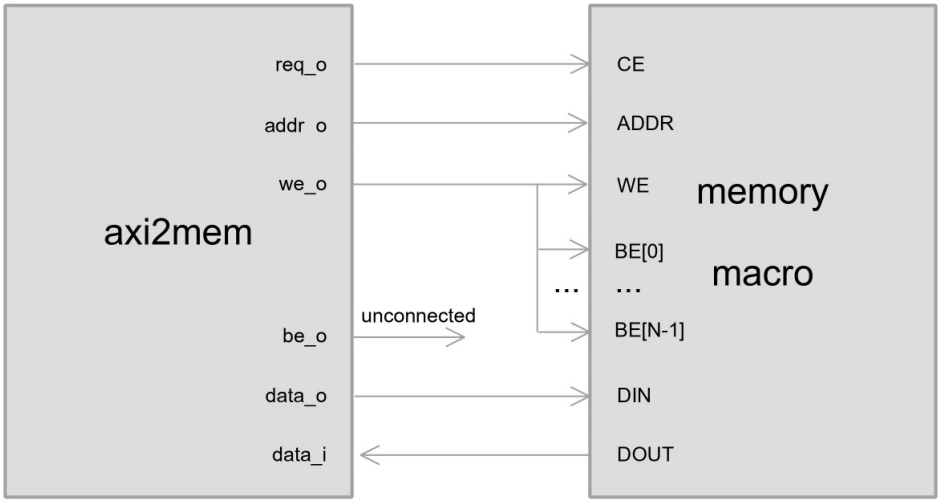

Figure 2: Block diagram

In configuration cases 1 and 2 the bit width of memory macro should be the same as bit width of the AXI4 data bus. In configuration case 3 the bit width of memory macro will always be different from bit width of the AXI4 data bus and will be as specified in the following table.

AXI4 data bus bit width	**Memory macro data bus bit width**
8	13
16	22
32	39
64	72
128	137
256	266
512	523

2.5 Scrubber

Scrubber is enabled if define ATM_SCRUBBER_EN is active. When scrubber is enabled there are scrubber-related registers that can be accessed via APB interface. If scrubber is turned on (ATM_SCRB_CR.EN=1) a timeout cycle starts at once and every time when scrubber completes its operation. Timeout cycle repeats infinitely until scrubber is turned off (ATM_SCRB_CR.EN=0). Every time when timeout period ends (internal counter becomes 0 after a series of decrements) the scrubber begins a run by all memory addresses. The timeout duration can be set up by writes to ATM_SCRB_T0 and ATM_SCRB_T1 registers.

During its run the scrubber reads every memory address and checks if there is a single error in this address. If there is a single error the scrubber gets fixed value from SECDED block output and writes it instead of corrupt value.

Scrubber run can be interrupted by AXI4 transaction. If scrubber run is interrupted then after every AXI4 transaction scrubber makes memory inaccessible for AXI4 interface for at least 2 or 3 cycles. It makes memory inaccessible for 2 cycles if there is no error in read data and for 3 cycles if there is error in read data. After these 2 or 3 cycles scrubber run can again be interrupted. This mechanism allows to share memory between AXI4 and scrubber.

Scrubber run can be forced by writing 1 to ATM_SCRB_CR.FR.

3 Registers

Offset	Register name
0x00	AXI4 to memory bridge control register ATM_CR
0x04	AXI4 to memory bridge status register ATM_SR
0x08	AXI4 to memory bridge last single error address register (LSB) ATM_LSEAR_LSB
0x0C	AXI4 to memory bridge last single error address register (MSB) ATM_LSEAR_MSB
0x10	AXI4 to memory bridge last double error address register (LSB) ATM_LDEAR_LSB
0x14	AXI4 to memory bridge last double error address register (MSB) ATM_LDEAR_MSB
0x100	AXI4 to memory bridge scrubber control register ATM_SCRB_CR
0x104	AXI4 to memory bridge scrubber timeout cycles register ATM_SCRB_T0
0x108	AXI4 to memory bridge scrubber timeout cycles register ATM_SCRB_T1

The following abbreviations are used in register descriptions:

RW - software can read and write to these bits.

RO - software can only read these bits.

WO - software can only write to this bit. Reading the bit returns the reset value.

RCW0 - Software can read as well as clear this bit by writing 0.

Register name: AXI4 to memory bridge control register ATM_CR

Address offset: 0x00

Bit count	Type	Reset value	Field	Bits	Description
1	RW	0	SECD	[0]	Disable single error correction. 0 - single errors are corrected. 1 - single errors are not corrected
1	RW	0	SEIE	[1]	Enable interrupt generation when single error is detected. 0 - interrupt generation disabled. 1 - interrupt generation enabled.
1	RW	0	DEIE	[2]	Enable interrupt generation when double error is detected. 0 - interrupt generation disabled. 1 - interrupt generation enabled.
29	RO	0..0b	reserved	[31:3]	Reserved for future use.

Register name: AXI4 to memory bridge status register ATM_SR

Address offset: 0x04

Bit count	Type	Reset value	Field	Bits	Description
1	RCW0	0	SEF	[0]	Single error flag. Set by hardware when single error is detected by SECDED blocks. Cleared only by software.
1	RCW0	0	DEF	[1]	Double error flag. Set by hardware when double error is detected by SECDED blocks. Cleared only by software.
30	RO	0..0b	reserved	[31:2]	Reserved for future use.

Register name: AXI4 to memory bridge last single error address register (LSB) ATM_LSEAR_LSB

Address offset: 0x08

Bit count	Type	Reset value	Field	Bits	Description
32	RO	00...0	LSEAR_LSB	[31:0]	Least significant bits of last single error address.

Register name: AXI4 to memory bridge last single error address register (MSB) ATM_LSEAR_MSB

Address offset: 0x0C

Bit count	Type	Reset value	Field	Bits	Description
32	RO	00...0	LSEAR_MSB	[31:0]	Most significant bits of last single error address.

Register name: AXI4 to memory bridge last double error address register (LSB) ATM_LDEAR_LSB

Address offset: 0x10

Bit count	Type	Reset value	Field	Bits	Description
32	RO	00...0	LDEAR_LSB	[31:0]	Least significant bits of last double error address.

Register name: AXI4 to memory bridge last double error address register (MSB) ATM_LDEAR_MSB

Address offset: 0x14

Bit count	Type	Reset value	Field	Bits	Description
32	RO	00...0	LDEAR_MSB	[31:0]	Most significant bits of last double error address.

Register name: AXI4 to memory bridge scrubber control register ATM_SCRB_CR

Address offset: 0x100

Bit count	Type	Reset value	Field	Bits	Description
1	WO	0	EN	[0]	Enable scrubber. 0 - scrubber disabled, 1 - scrubber enabled. When scrubber is enabled it runs through all memory addresses after every timeout period and fixes single errors when it detects them. Once this bit becomes 1 scrubber timeout countdown begins. Timeout countdown also begins when every scrubber run ends. Once this bit becomes 0 scrubber timeout counter is reset and scrubber run interrupts and next time starts from zero address.
1	WO	0	FR	[1]	Force scrubber run. When 1 is written to this bit scrubber begins a single run through all memory addresses. Don't set this bit to 1 together with EN bit.
30	RO	0..0b	reserved	[31:2]	Reserved for future use.

Register name: AXI4 to memory bridge scrubber timeout cycles register ATM_SCRB_T0

Address offset: 0x104

Bit count	Type	Reset value	Field	Bits	Description
32	RW	00...0	TIM_LSB	[31:0]	Least significant bits of scrubber timeout period in clock cycles.

Register name: AXI4 to memory bridge scrubber timeout cycles register ATM_SCRB_T1

Address offset: 0x108

Bit count	Type	Reset value	Field	Bits	Description
10	RW	00...0	TIM_MSB	[9:0]	Most significant bits of scrubber timeout period in clock cycles.
22	RO	0..0b	reserved	[31:10]	Reserved for future use.

4 Software source code example

Example code for this block is not provided.

5 Port descriptions

Name	Type	Description
clk	I	System clock.
rstn	I	System reset (active low).
req_o	O	Memory request (enable). When 1, memory will be read or written.
we_o	O	Memory write enable.
addr_o	O	Memory address.
be_o	O	Memory byte enable.
data_o	O	Data for memory.
data_i	I	Data from memory.
irq_s_o	O	Interrupt request when single error occurs (can be enabled by internal register). Interrput is level-triggered (the device holds it at active (HIGH) level until corresponding flag is cleared).
irq_d_o	O	Interrupt request when double error occurs (can be enabled by internal register). Interrput is level-triggered (the device holds it at active (HIGH) level until corresponding flag is cleared).
axi_*	Bus	AXI4 bus signals.
apb_*	Bus	APB bus signals (SECDED control and status).

6 Configuration options

AXI_DATA_WIDTH_8_USE_SECDED (define, file axi2mem_defs.sv) - AXI4 data width is 8 and SECDED will be used for data.

AXI_DATA_WIDTH_16_USE_SECDED (define, file axi2mem_defs.sv) - AXI4 data width is 16 and SECDED will be used for data.

AXI_DATA_WIDTH_32_USE_SECDED (define, file axi2mem_defs.sv) - AXI4 data width is 32 and SECDED will be used for data.

AXI_DATA_WIDTH_64_USE_SECDED (define, file axi2mem_defs.sv) - AXI4 data width is 64 and SECDED will be used for data.

AXI_DATA_WIDTH_128_USE_SECDED (define, file axi2mem_defs.sv) - AXI4 data width is 128 and SECDED will be used for data.

AXI_DATA_WIDTH_256_USE_SECDED (define, file axi2mem_defs.sv) - AXI4 data width is 256 and SECDED will be used for data.

AXI_DATA_WIDTH_512_USE_SECDED (define, file axi2mem_defs.sv) - AXI4 data width is 512 and SECDED will be used for data.

If none of the above defines enabled, then AXI4 data width will be as specified by AXI_DATA_WIDTH parameter and SECDED logic will not be inserted.

ATM_RMW_EN (define) - enable Read-Modify-Write sequence for write transfers. When defined, RAM without byte write enable can be used with axi2mem. This define is enabled automatically when any of *_USE_SECDED defines is enabled.

MEM_ADDR_WIDTH (parameter) - address width of the connected memory block.

AXI_ID_WIDTH (parameter) - width of AXI4 ID signals of all channels.

AXI_ADDR_WIDTH (parameter) - AXI4 address width.

AXI_DATA_WIDTH (parameter) - AXI4 data width.

START_ADDR (parameter) - this parameter is ignored when CHECK_ADDR_VALIDITY = 0. This is AXI4 address that will be used to access zero address of connected memory macro. log2(AXI_DATA_WIDTH/8) + MEM_ADDR_WIDTH least significant bits of this value must be 0s. Also see description of CHECK_ADDR_VALIDITY parameter.

CHECK_ADDR_VALIDITY (parameter) - When this parameter is set to 1, please specify START_ADDR parameter value. When this parameter is 1 and if address is out of memory range, slave will return RRESP = SLVERR or BRESP = SLVERR and exclusive access monitor (if enabled) will ignore transactions with out-of-range address. When this parameter is 0, AXI4 address validity is not checked and exclusive access monitor (if enabled) will not ignore address-out-of-range transactions.

EXCLUSIVE_ACCESS_EN (parameter) - when this parameter is 0, exclusive access (AxLOCK = 1 and EXOKAY response, see AXI4 specification, A7.2 "Exclusive accesses" section) is not supported, when 1 - the device includes exclusive access monitor that stores and checks exclusive access parameters and status for every ID and provides EXOKAY when necessary.

EXA_CHECK_INSTANT (parameter) - this parameter is ignored when EXCLUSIVE_ACCESS_EN = 0. This parameter defines exclusive access monitor implementation. When 0 exclusive access logic requires less gate count and has dereased internal reg-to-reg delays but maximum delay for write transactions is 256 x 2**AXI_ID_WIDTH cycles. When this parameter is 1 exclusive access logic requires more gate count and has increased internal reg-to-reg delays but all checks are performed instantly.

ATM_SCRUBBER_EN (parameter) - this parameter enables scrubber block as a part of AXI4 to memory bridge (scrubber is present when ATM_SCRUBBER_EN=1). This block periodically reads every memory address and fixes single errors when these are detected in read data. ATM_SCRUBBER_EN can only be enabled together with any of *_USE_SECDED enables.

MULTICYCLE_READ_N - number of additional cycles for multicycle read. If 0, then valid data appear 1 cycle after address is provided, if greater than 0 then valid data appear MULTICYCLE_READ_N+1 cycles after address is provided.